

SN65HVD178x-Q1 Fault-Protected RS-485 Transceivers with 3.3-V to 5-V Operation

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the Following Results
 - Device Temperature Grade 1:
 - 40°C to 125°C Ambient Operating Temperature Range
 - Device HBM ESD Classification Level H2
 - Device CDM ESG Classification Level C3B
- Bus-Pin Fault Protection to:
 - > ±70 V ('HVD1780, 81)
 - > ±30 V ('HVD1782)
- Operation With 3.3-V to 5-V Supply Range
- ±16 kV HBM Protection on Bus Pins
- Reduced Unit Load for up to 320 Nodes
- Failsafe Receiver for Open-Circuit, Short-Circuit and Idle-Bus Conditions
- Low Power Consumption
 - Low Standby Supply Current, 1 µA Max
 - I_{CC} 4-mA Quiescent During Operation
- Pin-Compatible With Industry-Standard SN75176
- Signaling Rates of 115 kbps, 1 Mbps, and up to 10 Mbps

2 Applications

Automotive Data Links

3 Description

These devices are designed to survive overvoltage faults such as direct shorts to power supplies, mis-wiring faults, connector failures, cable crushes, and tool mis-applications. They are also robust to ESD events, with high levels of protection to the human-body-model specification.

These devices combine a differential driver and a differential receiver, which operate from a single power supply. In the 'HVD1782, the driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. This port features a wide common-mode voltage range, making the devices suitable for multipoint applications over long cable runs. These devices are characterized from –40°C to 125°C. These devices are pin-compatible with the industry-standard SN75176 transceiver, making them drop-in upgrades in most systems.

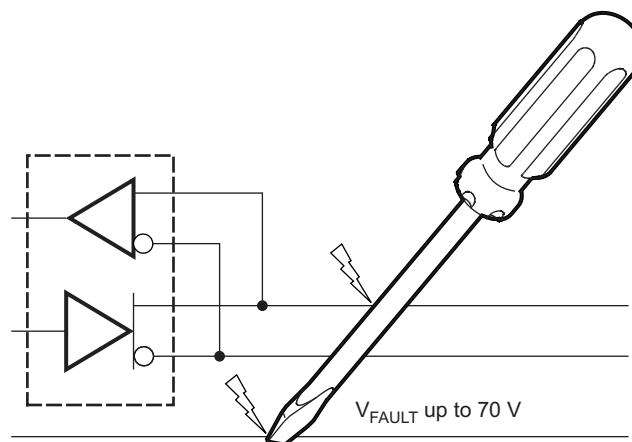
These devices are fully compliant with ANSI TIA/EIA 485-A with a 5-V supply and can operate with a 3.3-V supply with reduced driver output voltage for low-power applications. For applications where operation is required over an extended common-mode voltage range, see the SN65HVD1785 (SLLS872) data sheet.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVD1780-Q1, SN65HVD1781-Q1, SN65HVD1782-Q1	SOIC (8)	4.90 mm x 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Simplified Schematic



M0092-02



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (September 2010) to Revision A

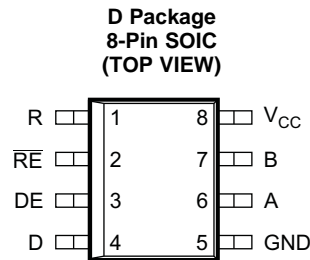
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- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section **1**
- Added new ListItem in Features, second one with sub list items..... **1**

5 Device Comparison Table

TRANSCEIVER	SIGNALING RATE	NUMBER OF NODES
HVD1780	Up to 115 kbps	Up to 320
HVD1781	Up to 1 Mbps	Up to 320
HVD1782	Up to 10 Mbps	Up to 64

6 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	6	Bus I/O	Driver output or receiver input (complementary to B)
B	7	Bus I/O	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable, active high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
\overline{RE}	2	Digital input	Receiver enable, active low
VCC	8	Supply	3.15-V-to-5.5-V supply

7 Specifications

7.1 Absolute Maximum Ratings

See Note ⁽¹⁾

			MIN	MAX	UNIT
V_{CC}	Supply voltage		-0.5	7	V
	Voltage range at bus pins	'HVD1780, 81	-70	70	V
		'HVD1782	-70	30	
	Input voltage range at any logic pin		-0.3	$V_{CC} + 0.3$	V
	Transient overvoltage pulse through 100 Ω per TIA-485		-70	70	V
	Receiver output current		-24	24	mA
T_J	Junction temperature			170	$^{\circ}\text{C}$
	Continuous total power dissipation		See Power Dissipation Ratings		

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT	
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	IEC 60749-26	Bus terminals and GND	±16000	V
			Test method based upon AEC-Q100-002	Bus terminals and GND	±16000	
			AEC-Q100-002	All pins	±4000	
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾		All pins	±2000	
		Machine Model (MM), AEC-Q100-003		All pins	±400	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT	
V_{CC}	Supply voltage	3.15	5	5.5	V	
V_I	Input voltage at any bus terminal (separately or common mode) ⁽¹⁾	-7		12	V	
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)	2		V_{CC}	V	
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)	0		0.8	V	
V_{ID}	Differential input voltage	-12		12	V	
I_O	Output current, driver	-60		60	mA	
	Output current, receiver	-8		8	mA	
R_L	Differential load resistance	54	60		Ω	
C_L	Differential load capacitance		50		pF	
$1/t_{UI}$	Signaling rate	HVD1780		115	Mbps	
		HVD1781		1		
		HVD1782		10		
T_A	Operating free-air temperature (See application section for thermal information)	5-V supply		-40	105	$^{\circ}\text{C}$
		3.3-V supply		-40	125	
T_J	Junction Temperature			-40	150	

(1) By convention, the least positive (most negative) limit is designated as minimum in this data sheet.

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN65HVD1781-Q1		UNIT	
		D (SOIC)			
		8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	JEDEC high-K model		138	$^{\circ}\text{C}/\text{W}$
		JEDIC low-K model		242	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance			61	$^{\circ}\text{C}/\text{W}$
$R_{\theta JB}$	Junction-to-board thermal resistance			62	$^{\circ}\text{C}/\text{W}$
Ψ_{JT}	Junction-to-top characterization parameter			3.8	$^{\circ}\text{C}/\text{W}$
Ψ_{JB}	Junction-to-board characterization parameter			38.6	$^{\circ}\text{C}/\text{W}$
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance			N/A	$^{\circ}\text{C}/\text{W}$

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
V _{OD}	Driver differential output voltage magnitude	R _L = 60 Ω, 4.75 V ≤ V _{CC} ≤ 3.75 V on each output to -7 V to 12 V, Figure 6	T _A < 85°C	1.5			V	
			T _A < 125°C	1.4				
		R _L = 54 Ω, 4.75 V ≤ V _{CC} ≤ 5.25 V	T _A < 85°C	1.7	2			
			T _A < 125°C	1.5				
		R _L = 54 Ω, 3.15 V ≤ V _{CC} ≤ 3.45 V		0.8	1			
R _L = 100 Ω, 4.75 V ≤ V _{CC} ≤ 5.25 V	T _A < 85°C	2.2	2.5					
	T _A < 125°C	2						
Δ V _{OD}	Change in magnitude of driver differential output voltage	R _L = 54 Ω		-50	0	50	mV	
V _{OC(SS)}	Steady-state common-mode output voltage			1	V _{CC} /2	3	V	
ΔV _{OC}	Change in differential driver output common-mode voltage			-50	0	50	mV	
V _{OC(PP)}	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors, See Figure 7			500		mV	
C _{OD}	Differential output capacitance				23		pF	
V _{IT+}	Positive-going receiver differential input voltage threshold				-100	-35	mV	
V _{IT-}	Negative-going receiver differential input voltage threshold			-180	-150			
V _{HYS}	Receiver differential input voltage threshold hysteresis (V _{IT+} - V _{IT-}) ⁽¹⁾			30	50			
V _{OH}	Receiver high-level output voltage	I _{OH} = -8 mA		2.4	V _{CC} - 0.3		V	
V _{OL}	Receiver low-level output voltage	I _{OL} = 8 mA	T _A < 85°C		0.2	0.4	V	
			T _A < 125°C			0.5		
I _{I(LOGIC)}	Driver input, driver enable, and receiver enable input current			-50		50	μA	
I _{OZ}	Receiver output high-impedance current	V _O = 0 V or V _{CC} , \overline{RE} at V _{CC}		-1		1	μA	
I _{OS}	Driver short-circuit output current			-200		200	mA	
I _{I(BUS)}	Bus input current (disabled driver)	V _{CC} = 3.15 to 5.5 V or V _{CC} = 0 V, DE at 0 V	V _I = 12 V	1780, 1781		75	100	μA
				1782		400	500	
			V _I = -7 V	1780, 1781		-60	-40	
				1782		-400	-300	
I _{CC}	Supply current (quiescent)	Driver and receiver enabled	DE = V _{CC} , RE = GND, no load		4	6	mA	
		Driver enabled, receiver disabled	DE = V _{CC} , RE = V _{CC} , no load		3	5		
		Driver disabled, receiver enabled	DE = GND, RE = GND, no load		2	4		
		Driver and receiver disabled, standby mode	DE = GND, D = open, RE = V _{CC} , no load, T _A < 85°C		0.15	1	μA	
DE = GND, D = open, RE = V _{CC} , no load, T _A < 125°C					12			
Supply current (dynamic)		See the Typical Characteristics section						

(1) Ensured by design. Not production tested.

7.6 Power Dissipation Ratings

PARAMETER	TEST CONDITIONS	VALUE	UNIT
P _D Power dissipation	V _{CC} = 3.6V, T _J = 150°C, R _L = 300 Ω, C _L = 50 pF (driver), C _L = 15 pF (receiver) 3.3-V supply, unterminated ⁽¹⁾	75	mW
	V _{CC} = 3.6V, T _J = 150°C, R _L = 100 Ω, C _L = 50 pF (driver), C _L = 15 pF (receiver) 3.3-V supply, RS-422 load ⁽¹⁾	95	
	V _{CC} = 3.6V, T _J = 150°C, R _L = 54 Ω, C _L = 50 pF (driver), C _L = 15 pF (receiver) 3.3-V supply, RS-485 load ⁽¹⁾	115	
	V _{CC} = 5.5V, T _J = 150°C, R _L = 300 Ω, C _L = 50 pF (driver), C _L = 15 pF (receiver) 5-V supply, unterminated ⁽¹⁾	290	
	V _{CC} = 5.5V, T _J = 150°C, R _L = 100 Ω, C _L = 50 pF (driver), C _L = 15 pF (receiver) 5-V supply, RS-422 load ⁽¹⁾	320	
	V _{CC} = 5.5V, T _J = 150°C, R _L = 54 Ω, C _L = 50 pF (driver), C _L = 15 pF (receiver) 5-V supply, RS-485 load ⁽¹⁾	400	
T _{SD} Thermal-shutdown junction temperature		170	°C

(1) Driver and receiver enabled, 50% duty cycle square-wave signal at signaling rate: 1 Mbps.

7.7 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
DRIVER (HVD1780)							
t_r, t_f	Driver differential output rise/fall time	$R_L = 54 \Omega$, $C_L = 50 \text{ pF}$, See Figure 8	$3.15 \text{ V} < V_{CC} < 3.45 \text{ V}$	0.4	1.4	1.8	μs
			$3.15 \text{ V} < V_{CC} < 5.5 \text{ V}$	0.4	1.7	2.6	μs
t_{PHL}, t_{PLH}	Driver propagation delay			0.8	2	μs	
$t_{SK(P)}$	Driver differential output pulse skew, $ t_{PHL} - t_{PLH} $			20	250	ns	
t_{PHZ}, t_{PLZ}	Driver disable time			0.1	5	μs	
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled	See Figure 9 and Figure 10		0.2	3	μs
		Receiver disabled			3	12	μs
DRIVER (HVD1781)							
t_r, t_f	Driver differential output rise/fall time	$R_L = 54 \Omega$, $C_L = 50 \text{ pF}$, See Figure 8		50	300	ns	
t_{PHL}, t_{PLH}	Driver propagation delay				200	ns	
$t_{SK(P)}$	Driver differential output pulse skew, $ t_{PHL} - t_{PLH} $				25	ns	
t_{PHZ}, t_{PLZ}	Driver disable time				3	μs	
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled	See Figure 9 and Figure 10		300	ns	
		Receiver disabled			10	μs	
DRIVER (HVD1782)							
t_r, t_f	Driver differential output rise/fall time	$R_L = 54 \Omega$, $C_L = 50 \text{ pF}$	All V_{CC} and Temp		50	ns	
			$V_{CC} > 4.5 \text{ V}$ and $T < 105^\circ\text{C}$		16		
t_{PHL}, t_{PLH}	Driver propagation delay					55	ns
$t_{SK(P)}$	Driver differential output pulse skew, $ t_{PHL} - t_{PLH} $		See Figure 8		10	ns	
t_{PHZ}, t_{PLZ}	Driver disable time				3	μs	
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled	See Figure 9 and Figure 10		300	ns	
		Receiver disabled			9	μs	
RECEIVER (ALL DEVICES UNLESS OTHERWISE NOTED)							
t_r, t_f	Receiver output rise/fall time ⁽¹⁾	$C_L = 15 \text{ pF}$, See Figure 11	All devices	4	15	ns	
t_{PHL}, t_{PLH}	Receiver propagation delay time		HVD1780, HVD1781	100	200	ns	
			HVD1782		80		
$t_{SK(P)}$	Receiver output pulse skew, $ t_{PHL} - t_{PLH} $		HVD1780, HVD1781	6	20	ns	
			HVD1782		5		
t_{PLZ}, t_{PHZ}	Receiver disable time ⁽¹⁾	Driver enabled, See Figure 12		15	100	ns	
$t_{PZL(1)}, t_{PZH(1)}$ $t_{PZL(2)}, t_{PZH(2)}$	Receiver enable time	Driver enabled, See Figure 12		80	300	ns	
		Driver disabled, See Figure 13		3	9	μs	

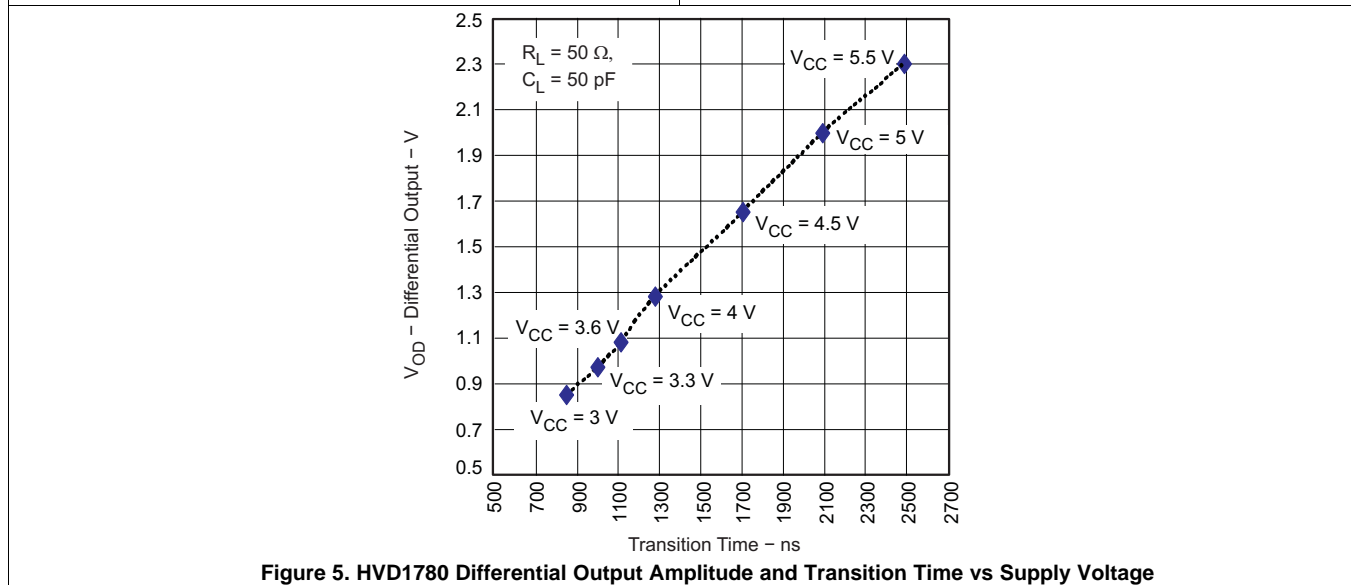
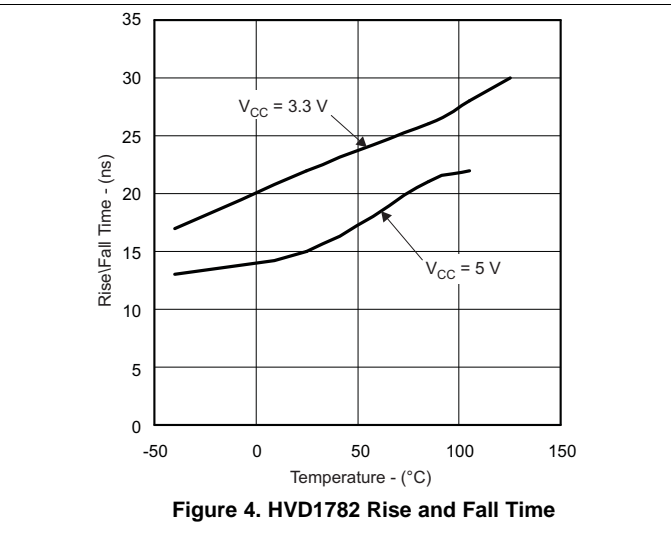
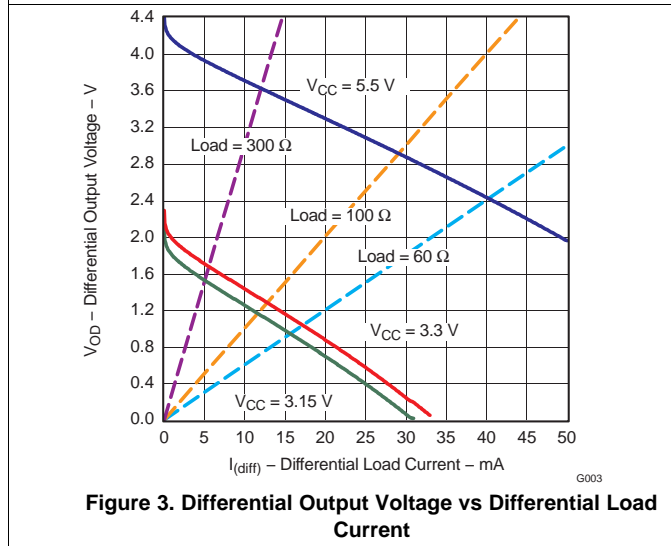
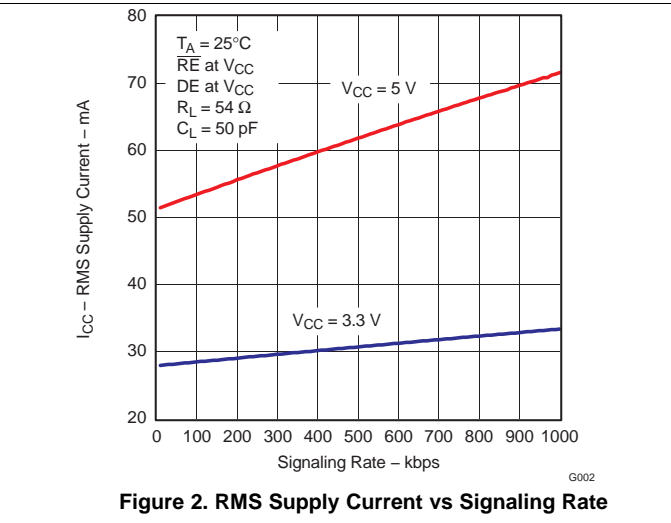
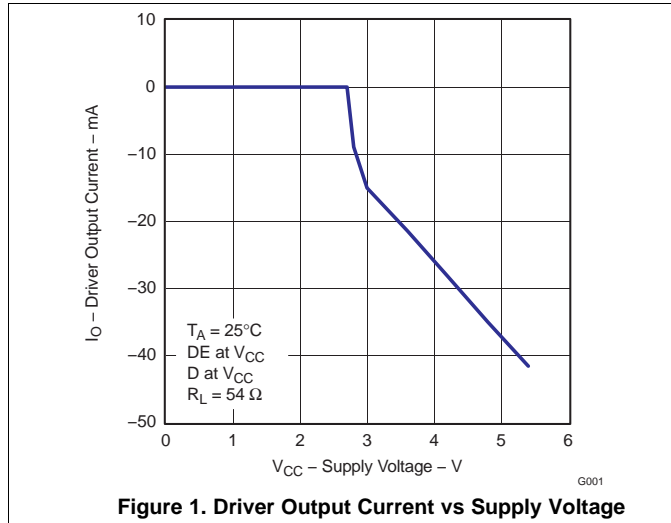
(1) Ensured by design. Not production tested.

7.8 Package Dissipation Ratings

PACKAGE ⁽¹⁾	JEDEC THERMAL MODEL	$T_A < 25^\circ\text{C}$ RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}$	$T_A = 85^\circ\text{C}$ RATING	$T_A = 105^\circ\text{C}$ RATING	$T_A = 125^\circ\text{C}$ RATING (3.3 V ONLY)
SOIC (D) 8-pin	High-K	905 mW	7.25 mW/ $^\circ\text{C}$	470 mW	325 mW	180 mW
	Low-K	516 mW	4.1 mW/ $^\circ\text{C}$	268 mW	186 mW	103 mW

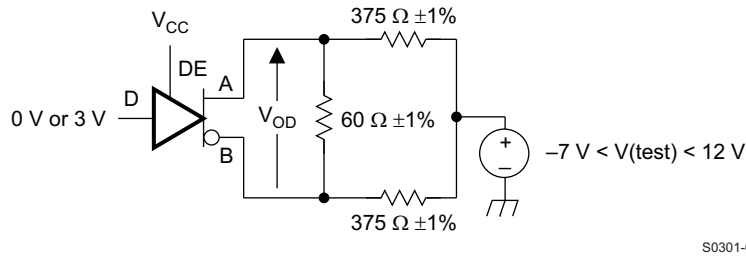
 (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

7.9 Typical Characteristics



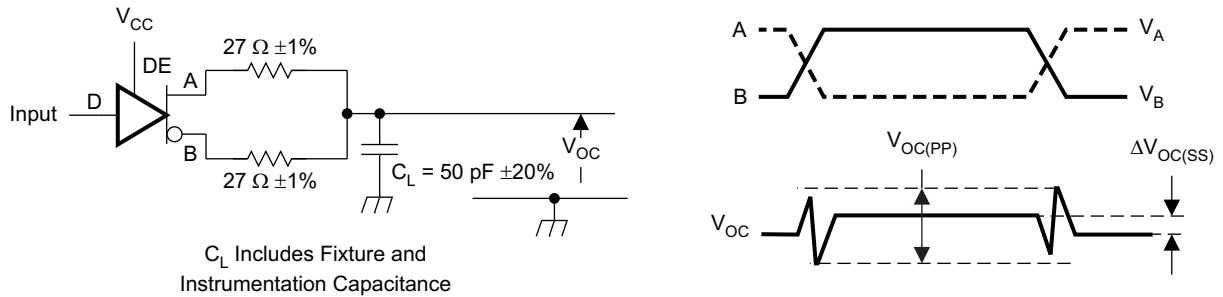
8 Parameter Measurement Information

Input generator rate is 100 kbps, 50% duty cycle, rise and fall times less than 6 nsec, output impedance 50 Ω.



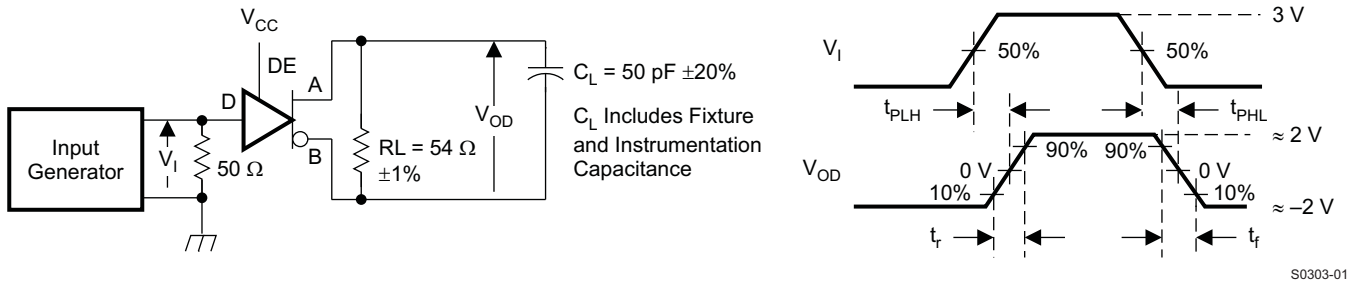
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Figure 6. Measurement of Driver Differential Output Voltage With Common-Mode Load



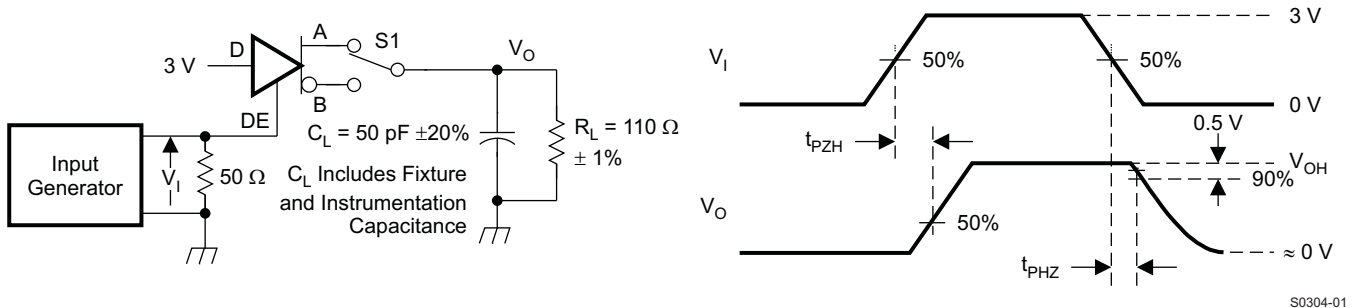
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Figure 7. Measurement of Driver Differential and Common-Mode Output With RS-485 Load



S0303-01

Figure 8. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



S0304-01

NOTE: D at 3 V to test non-inverting output, D at 0 V to test inverting output.

Figure 9. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load

Parameter Measurement Information (continued)

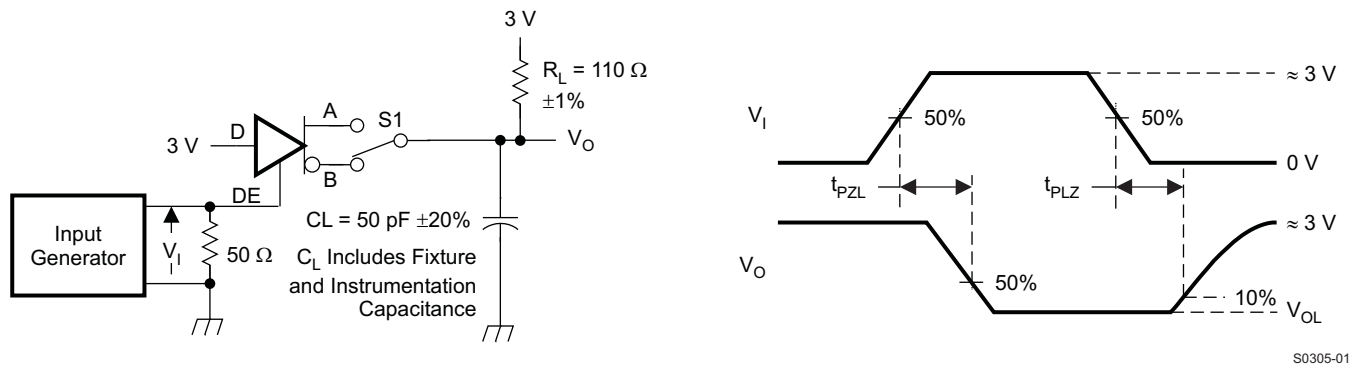


Figure 10. Measurement of Driver Enable and Disable Times With Active-Low Output and Pullup Load

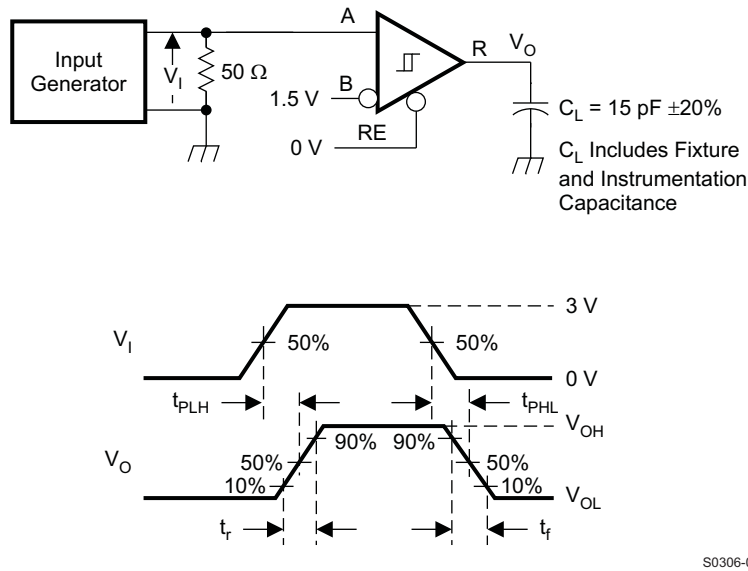
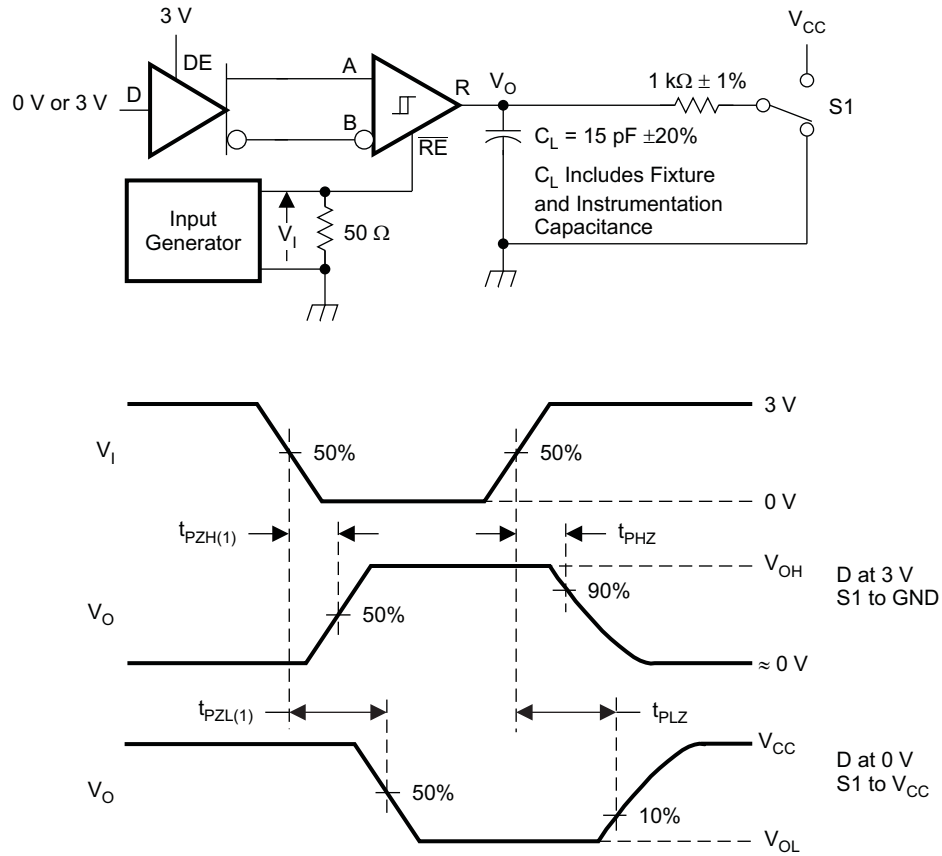


Figure 11. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

Parameter Measurement Information (continued)



S0307-01

Figure 12. Measurement of Receiver Enable/Disable Times With Driver Enabled

Parameter Measurement Information (continued)

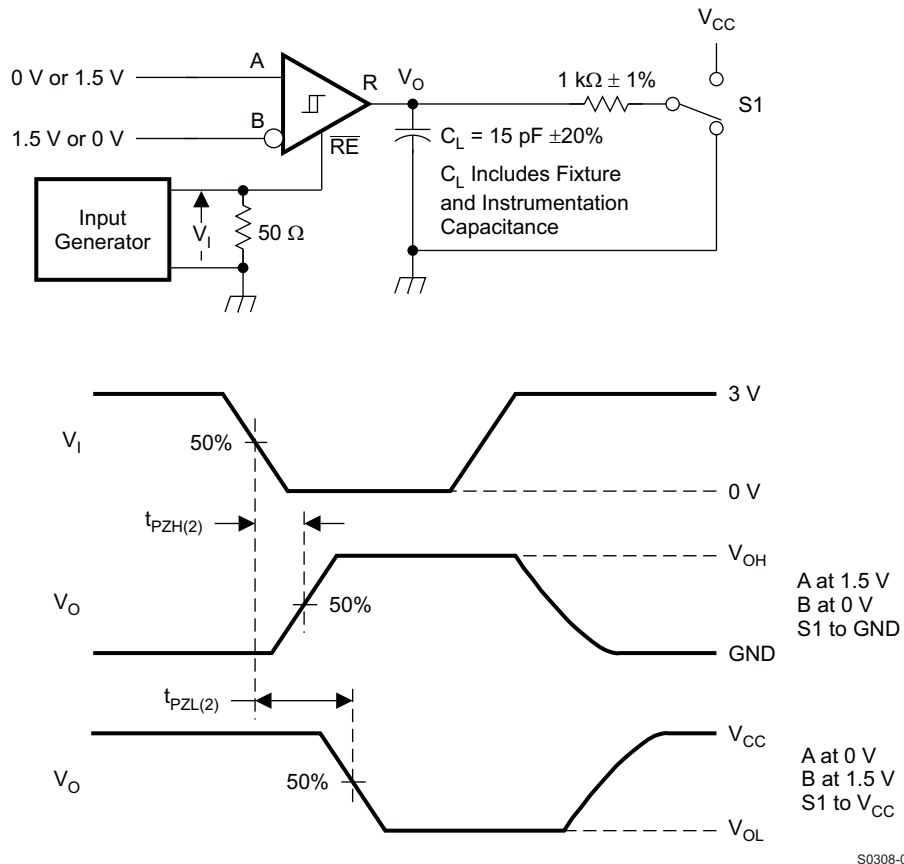


Figure 13. 'HVD1781 Measurement of Receiver Enable Times With Driver Disabled

9 Detailed Description

9.1 Overview

The SN65HVD1780, HVD1781, and HVD1782 are half-duplex RS-485 transceivers with available in three speed grades suitable for data transmission up to 115kbps, 1Mbps, and 10Mbps.

These devices feature a wide common-mode operating range and bus-pin fault protection up to $\pm 70V$. Each device has an active-high driver enable and active-low receiver enable. A standby current of less than $1\mu A$ can be achieved by disabling both driver and receiver.

9.2 Functional Block Diagram

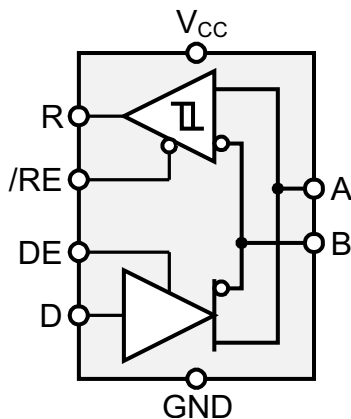


Figure 14. Logic Diagram (Positive Logic)

9.3 Feature Description

Internal ESD protection circuits protect the transceiver bus terminals against ± 16 kV Human Body Model (HBM) electrostatic discharges.

Device operation is specified over a wide temperature range from $-40^{\circ}C$ to $125^{\circ}C$.

9.3.1 Bus Fault Conditions

The SN65HVD178x family of RS-485 transceivers is designed to survive bus pin faults up to $\pm 70V$. The SN65HVD1782 will not survive a bus pin fault with a direct short to voltages above 30V when:

- The device is powered on, AND
- The driver is enabled (DE = HIGH), AND
 - D = HIGH AND the bus fault is applied to the A pin, OR
 - D = LOW AND the bus fault is applied to the B pin

Feature Description (continued)

Under other conditions, the device will survive shorts to bus pin faults up to $\pm 70V$. [Table 1](#) summarizes the conditions under which the device may be damaged, and the conditions under which the device will not be damaged.

Table 1. Bus Fault Conditions for the HVD1782

POWER	DE	D	A	B	RESULTS
OFF	X	X	$-70V < V_A < 70V$	$-70V < V_B < 70V$	Device survives
ON	LO	X	$-70V < V_A < 70V$	$-70V < V_B < 70V$	Device survives
ON	HI	L	$-70V < V_A < 70V$	$-70V < V_B < 30V$	Device survives
ON	HI	L	$-70V < V_A < 70V$	$30V < V_B$	Damage may occur
ON	HI	H	$-70V < V_A < 30V$	$-70V < V_B < 30V$	Device survives
ON	HI	H	$30V < V_A$	$-70V < V_B < 30V$	Damage may occur

9.3.2 Receiver Failsafe

The SN65HVD178x family of half-duplex transceivers provides internal biasing of the receiver input thresholds in combination with large input-threshold hysteresis. At a positive input threshold of $V_{IT+} = -35mV$ and an input hysteresis of $V_{HYS} = 30mV$, the receiver output remains logic high under bus-idle, bus-short, or open bus conditions in the presence of up to $130mV_{PP}$ differential noise without the need for external failsafe biasing resistors.

9.3.3 Hot-Plugging

These devices are designed to operate in “hot swap” or “hot-pluggable” applications. Key features for hot-pluggable applications are power-up and power-down glitch free operation, default disabled input and output pins, and receiver failsafe.

As shown in [Figure 14](#), an internal power-on reset circuit keeps the driver outputs in a high impedance state until the supply voltage has reached a level at which the device will reliably operate. This ensures that no problems will occur on the bus pin outputs as the power supply turns on or off.

As shown in [Device Functional Modes](#), the driver and receiver enable inputs (DE and \overline{RE}) are disabled by default. This ensures that the device will neither drive the bus nor report data on the R pin until the associated controller actively drivers the enable pins.

9.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pull-down resistor to ground, thus when left open the driver is disabled (high-impedance) by default. The D pin has an internal pull-up resistor to V_{CC} , thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 2. Driver Function Table

INPUT	ENABLE	OUTPUTS		DRIVER STATE
		A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus High by default

When the receiver enable pin, \overline{RE} , is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold, V_{IT+} , the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, V_{IT-} , the receiver output, R, turns low. If V_{ID} is between V_{IT+} and V_{IT-} the output is indeterminate.

When \overline{RE} is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

Table 3. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	RECEIVER STATE
$V_{ID} = V_A - V_B$	\overline{RE}	R	
$V_{ID} < V_{IT+}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output
Idle (terminated) bus	L	H	Fail-safe high output

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN65HVD1780, HVD1781, and HVD1782 are half-duplex RS-485 transceivers commonly used for asynchronous data transmissions. The driver and receiver enable pins allow for the configuration of different operating modes.

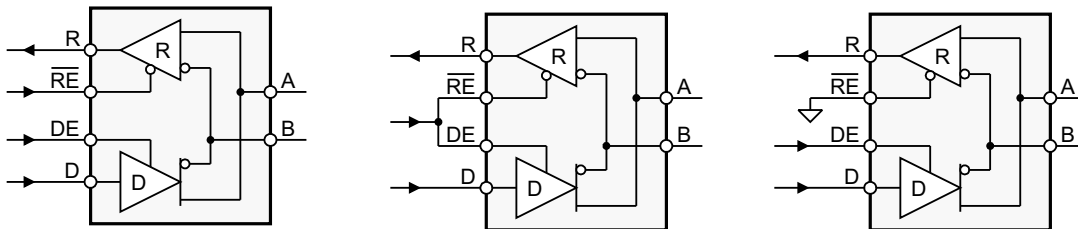


Figure 15. Half-Duplex Transceiver Configurations

Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high, and as a receiver when the direction-control line is low.

Additionally, only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node not only receives the data from the bus, but also the data it sends and can verify that the correct data have been transmitted.

10.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T , whose value matches the characteristic impedance, Z_0 , of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

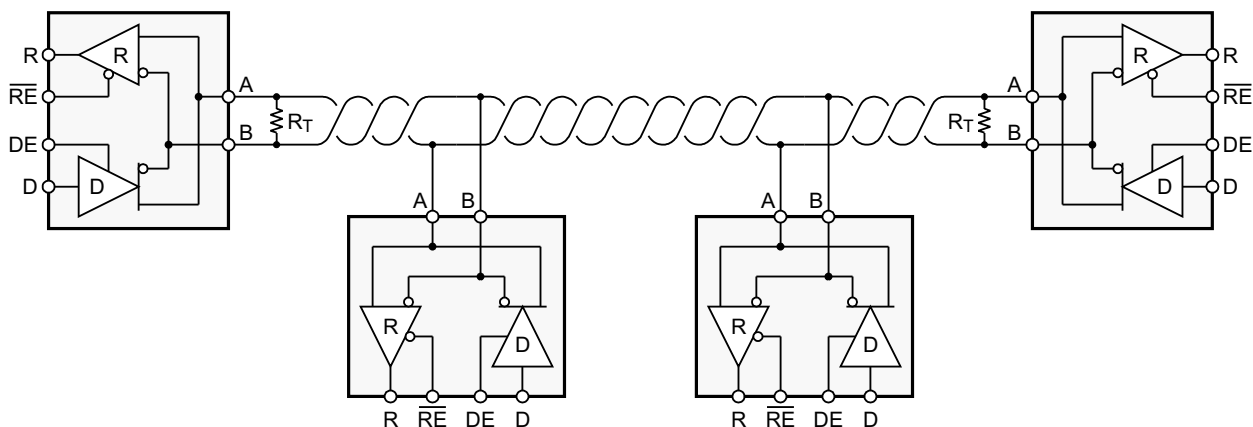


Figure 16. Typical RS-485 Network With Half-Duplex Transceivers

Typical Application (continued)

10.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

10.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length, meaning the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable may be without introducing data errors. While most RS-485 systems use data rates between 10kbps and 100kbps, some applications require data rates up to 250kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

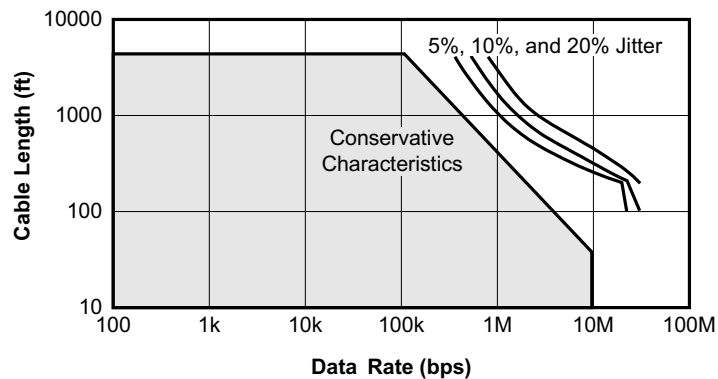


Figure 17. Cable Length vs Data Rate Characteristic

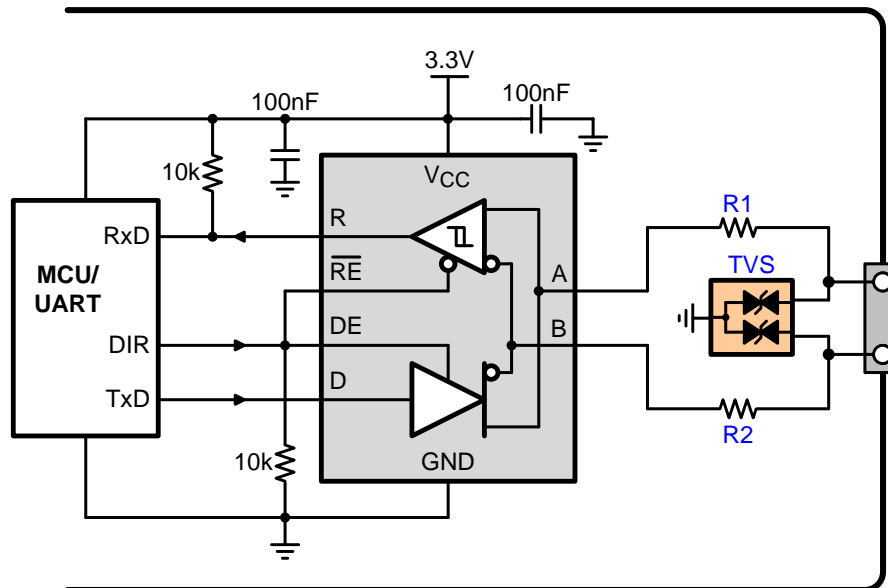
10.2.1.2 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12kΩ. Because the SN65HVD7x family consists of 1/10 UL transceivers, it is possible to connect up to 320 receivers to the bus.

10.2.2 Detailed Design Procedure

Although the SN65HVD178x-Q1 family is internally protected against human-body-model ESD strikes up to 16 kV, additional protection against higher-energy transients can be provided at the application level by implementing external protection devices.

Figure 18 shows a protection circuit intended to withstand 8-kV IEC ESD (per IEC 61000-4-2) as well as 4-kV EFT (per IEC 61000-4-4).

Typical Application (continued)

Figure 18. RS-485 Transceiver with External Transient Protection
Table 4. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	RS-485 Transceiver	SN65HVD178x-Q1	TI
R1, R2	10Ω, Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 600W Transient Suppressor	SMBJ43CA	Littlefuse

10.2.2.1 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{\text{stub}} \leq 0.1 \times t_r \times v \times c \quad (1)$$

Where:

t_r is the 10/90 rise time of the driver

c is the speed of light (3×10^8 m/s)

v is the signal velocity of the cable or trace as a factor of c

10.2.2.2 Receiver Failsafe

The differential receivers of the SN65HVD178x family are “failsafe” to invalid bus states caused by:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic High state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the “input indeterminate” range does not include zero volts differential. In order to comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input V_{ID} is more positive than +200mV, and must output a Low when V_{ID} is more negative than -200mV. The receiver parameters which determine the failsafe performance are $V_{IT(+)}$, $V_{IT(-)}$, and V_{HYS} (the separation between $V_{IT(+)}$ and $V_{IT(-)}$). As shown in the [Electrical Characteristics](#) table, differential signals more negative than -200mV will always cause a Low receiver output, and differential signals more positive than +200mV will always cause a High receiver output.

When the differential input signal is close to zero, it is still above the maximum $V_{IT(+)}$ threshold of -35mV, and the receiver output will be High. Only when the differential input is more than V_{HYS} below $V_{IT(+)}$ will the receiver output transition to a Low state. Therefore, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value, V_{HYS} , as well as the value of $V_{IT(+)}$.

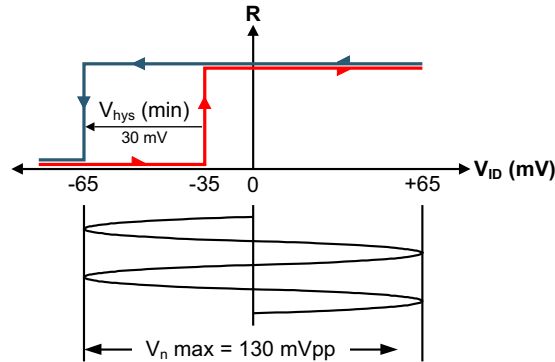
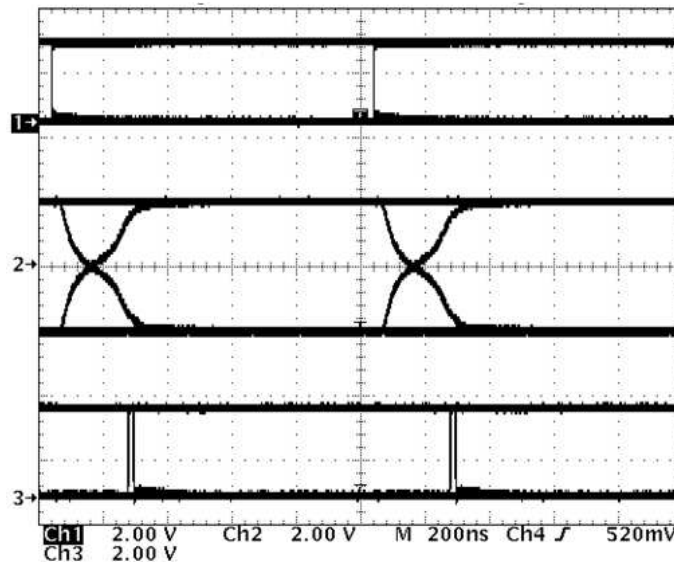


Figure 19. SN65HVD178x Noise Immunity Under Bus Fault Conditions

10.2.3 Application Curve



SN65HVD1781-Q1 D Input (Top)
Differential Output (Middle)
R Output (Bottom)

Figure 20. SN65HVD1781-Q1 PRBS Data Pattern — 1 Mbps Operation

11 Power Supply Recommendations

To assure reliable operation at all data rates and supply voltages, each supply should be buffered with a 100 nF ceramic capacitor located as close to the supply pins as possible. The TPS76350 is a linear voltage regulator suitable for the 5V supply.

12 Layout

On-chip IEC-ESD protection is good for laboratory and portable equipment but often insufficient for EFT and surge transients occurring in industrial environments. Therefore robust and reliable bus node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design.

12.1 Layout Guidelines

1. Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
2. Use V_{CC} and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100nF to 220nF bypass capacitors as close as possible to the V_{CC} pins of the transceiver, UART, or controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
6. Use 1k to 10k pull-up/down resistors for enable lines to limit noise currents in these lines during transient events.
7. While pure TVS protection is sufficient for surge transients up to 1kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

12.2 Layout Example

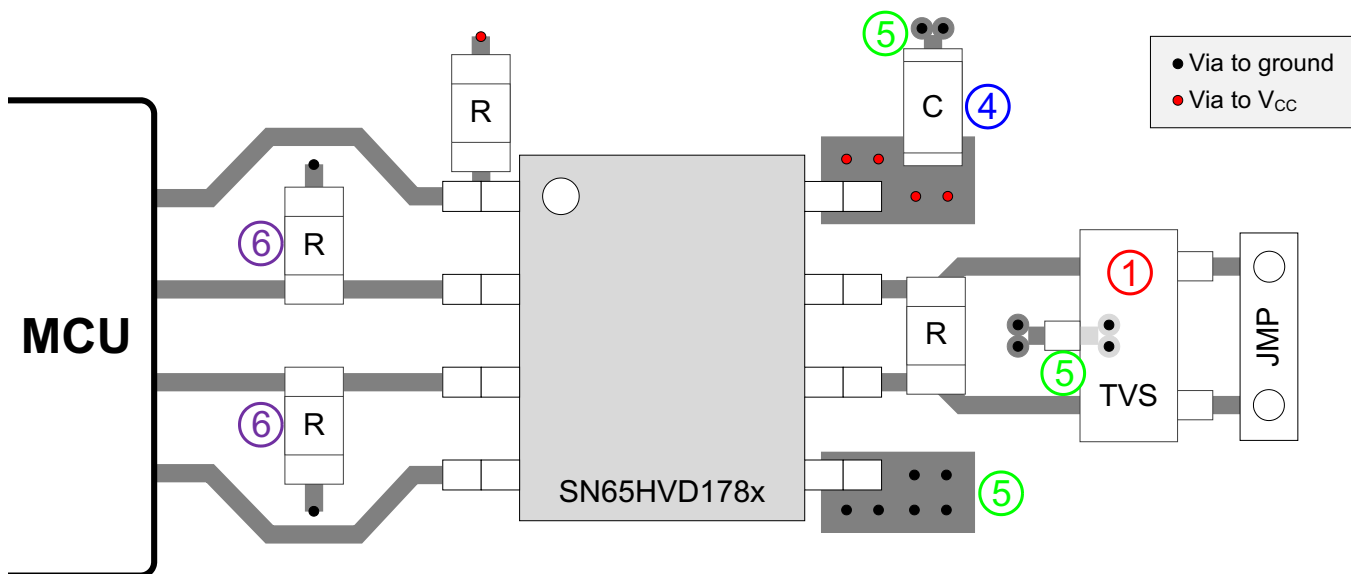


Figure 21. SN65HVD178x Half-Duplex Layout Example

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

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13.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD1780QDQ1	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI			
SN65HVD1780QDRQ1	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1780Q	
SN65HVD1781QDRQ1	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1781Q	Samples
SN65HVD1782QDQ1	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI			
SN65HVD1782QDRQ1	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	1782Q	

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN65HVD1780-Q1, SN65HVD1781-Q1, SN65HVD1782-Q1 :

- Catalog: [SN65HVD1780](#), [SN65HVD1781](#), [SN65HVD1782](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1781QDRQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1781QDRQ1	SOIC	D	8	2500	367.0	367.0	35.0

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040047-3/M 06/11

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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